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3. Nature of conveyance/Execution Date(s):

Execution Date(s) 10/27/2008

☒ Assignment   ☐ Merger

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4. Application number(s) or patent number(s):   ☐ This document is being filed together with a new application.

A. Patent Application No.(s)
See Attached Exhibit "A"

B. Patent No.(s)
See Attached Exhibit "A"

Additional numbers attached? ☒ Yes ☐ No

5. Name and address to whom correspondence concerning document should be mailed: Name: Christopher C. Winslade Internal Address: _____ Street Address: 500 West Madison Street 34th Floor City: Chicago State: Illinois Zip: 60661 Phone Number : 312-775-8000 Fax Number: 312-775-8100 Email Address: mhmpto@mcandrews-ip.com	**6. Total number of applications and patents involved:** 117 **7. Total fee** (37 CFR 1.21(h) & 3.41) $ 4680.00 ☐ Authorized to be charged by credit card ☒ Authorized to be charged to deposit account ☐ Enclosed ☐ None required (government interest not affecting title) **8. Payment Information** a. Credit Card Last 4 Numbers _____ Expiration Date _____ b. Deposit Account Number 13-0017 Authorized User Name McAndrews, Held & Malloy

9. Signature :   /Christopher C. Winslade/   December 17, 2008

Signature   Date
Christopher C. Winslade   Total number of pages including cover
Name of Person Signing   sheet, attachments, and documents   11

Title	Application Number/ Filing Date	Pub. No./ Patent No.	Pub. Date/ Issue Date
Remote-control device with directional audio system	11/839,798 08/16/07		
System and Method for Transferring a Multidimensional Array of Data to a Non-Contiguous Buffer	11/451,322 06/13/06	US 2008/0005499	01/03/08
A system and method of feature emphasis and de-emphasis in image processing	61/071,645		
Method and Apparatus for Managing Tasks in a Multiprocessor System	10/939,804 09/13/04	2006/0059484 A1	03/16/06
SIMD Processor with Register Addressing, Buffer Stall and Methods	10/929,992 08/30/04	2006/0047937 A1	03/02/06
SIMD Processor with Register Addressing, Buffer Stall and Methods	12/231,336 08/29/08		
Trellis Decoder for Decoding Data Stream including Symbols Coded with Multiple Convolutional Codes	10/973,486 10/26/04	2006/0088119 A1	04/27/06
SIMD Processor having Enhanced Operand Storage Interconnects	10/940,150 09/13/04	2006/0095712 A1	05/04/06
SIMD Processor Executing Min/Max Instructions	10/940,123 09/13/04	2006/0095739	05/04/06
SIMD Processor Executing Min/Max Instructions	12/231,891 09/05/08		
Digital Receiver Having Adaptive Carrier Recovery Circuit	10/757,536 01/15/04	7,342,981	03/11/08

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Title	Application Number/ Filing Date	Pub. No./ Patent No.	Pub. Date/ Issue Date
Audio/Video Separator	10/812,279 03/29/04	2005/0212977 A1	09/29/05
Worldwide Analog Television Signal Receiver	10/940,153 09/13/04	7,394,500	07/01/08
Film-Mode (3:2/2:2 Pulldown) Detector, Method and Video Device	10/837,835 05/03/04	2005/0243215	11/03/05
Low Latency Digital Filter and Method	11/090,478 03/25/05	2006/0215746	09/28/06
Method and Apparatus for Using the Host-Pod Interface of a Digital Television or Other Digital Audio/Video Receiver for New Services	11/306,317 12/22/05	2007/0146542 A1	06/28/07
Methods and Apparatus for Processing Variable Length Coded Data	11/046,048 01/28/05	7,132,963	11/07/06
Methods and Apparatus for Processing Variable Length Coded Data	11/538,336 10/03/06	7,385,534	06/10/08
Methods and Apparatus for Processing Variable Length Coded Data	12/133,489 06/05/2008		
Video Receiver Providing Video Attributes with Video Data	11/402,902 04/13/06	2007/0262979 A1	11/15/07
Image Analyser and Adaptive Image Scaling Circuit and Methods	11/619,358 01/03/07		
Enhanced Video Processing Using Motion Vector Data	12/032,796 02/28/08		
Low Latency Cadence Detection for Frame Rate Conversion	11/616,192 12/26/06	2008/0151109 A1	06/26/08

Title	Application Number/ Filing Date	Pub. No./ Patent No.	Pub. Date/ Issue Date
Video Processor Architecture and Method for Frame Rate Conversion	11/616,188 12/26/06	2008/0151108 A1	06/26/08
Harmonic Edge Synthesizer, Enhancer and Methods	11/619,366 01/03/07	2007/0152991 A1	07/05/07
Device and Methods for Reducing Visual Artifacts in Color Images	11/848,366 08/31/07		
Adaption of Frame Rate Converter Output Target Display Times Based on Video Content Detection	61/071,470 04/30/08		
Apparatus and Method for Synchronizing an SCDMA Upstream or any other...	09/074,036 05/06/98	6,243,369	06/05/01
Apparatus and Method for Synchronizing an SCDMA Upstream...	09/798,845 03/01/01	6,353,604 B2	030/5/02
Two Dimensional Interleave Process for CDMA...	09/152,643 09/14/98	6,466,564	10/15/02
Mixed DOCSIS 1.0 TDMA Burst with SCDMA...	09/337,167 06/21/99	6,459,703	10/01/02
Method and Apparatus for Faster Block Size...	09/648,278 08/23/00	6,848,036	01/25/05
Method and Apparatus to Improve SCDMA...	09/974,202 10/09/01	7,002,899 B2	02/21/06

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Title	Application Number/ Filing Date	Pub. No./ Patent No.	Pub. Date/ Issue Date
Method and Apparatus to Improve SCDMA...	11/326,225 01/04/06		
Down-Stream Transmitter and Cable...	10/944,962 09/18/04	20060085727	04/20/06
Downstream transmitter and cable modem receiver for 1024 QAM	12/286,337 09/29/08		
Blind Cost Criterion Timing Recovery	09/761,303 01/17/01	6,985,549	01/10/06
Carrier Phase Estimation Based On Single-Axis Constant Modulus Cost Criterion And Bussgang Criteria	09/922,006 08/03/01	7,031,405	04/18/06
Linear Prediction Based Initialization of A Single-Axis Blind Equalizer for VSB Modulations	10/016,665 12/11/01	7,027,500	04/11/06
DC Offset Correction For Constant Modulus Equalization	10/213,854 08/07/02	7,349,469	03/25/08
Rate Control for Digital Video Compression Processing	11/049,103 02/02/05	US-2006-0171457-A1	08/03/06
Picture adjustment methods and apparatus for image display device	11/504,496 08/15/06	20080043031A1	2/21/08
Method of estimating trellis encoded symbols utilizing simplified trellis decoding	09/099,730 06/19/98	6,178,209	01/23/01
Reduced complexity equalizer for multi mode signaling	09/100,705 06/19/98	6,426,972	07/30/02
Data slicer for combined trellis decoding and equalization	09/716,651 11/20/00	6,850,563	02/01/05

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Title	Application Number/ Filing Date	Pub. No./ Patent No.	Pub. Date/ Issue Date
Dual loop automatic gain control	10/253,245 09/24/02	7,116,955	10/3/06
Vertex data processing with multiple threads of execution	09/632,759 8/4/00	6,963,347	11/8/05
Vertex data processing with multiple threads of execution	11/250,754 10/14/05	US 2006-0033757 A1	02/16/06
Memory request interlock	09/638,550 8/14/00	6,810,470	10/26/04
Method and apparatus for detecting and correcting modulated signal impairments (phase noise)	11/947,090 11/29/07	US-2008-0123788- A1	05/29/08
Method and apparatus for detecting and correcting modulated signal impairments (burst noise)	11/947,124 11/29/07	US-2008-0123787- A1	05/29/08
Method and apparatus for detecting and correcting modulated signal impairments (gain noise)	11/947,105 11/29/07	US-2008-0123786- A1	05/29/08
Method to detect and mitigate impulse noise on receivers	11/775,836 7/10/07		
Framebuffer sharing for video processing	11/847,802 08/30/07	US-2008-0165287- A1	07/10/08
High performance embedded memory and I/O bridge design in SOC	11/871,120 10/11/07		
Method and system for motion compensated noise reduction	11/847,820 08/30/07	US-2008-0055477- A1	03/06/08
Unified memory architecture for T-CON end back-end video processor ICS (Integrated Circuits)	11/874,659 10/18/07	US-2008-0198937- A1	08/21/08

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Title	Application Number/ Filing Date	Pub. No./ Patent No.	Pub. Date/ Issue Date
Halo artifact removal method	11/960,991 12/20/07		
Method and apparatus for impulse noise detection and suppression for DVB-T	11/964,373 12/26/07		
Method and apparatus for reduced complexity video processing via special chroma handling	12/126,321 05/23/08		
H.264 data processing	11/897,714 08/30/07	US-2008-0165860- A1	07/10/08
Video stream timing detection	11/839,361 08/15/07	US-2008-0143876- A1	06/19/08
Video decoder block	11/847,879 08/30/07	US-2008-0056357- A1	03/6/08
Neighboring context management	11/842,901 08/21/07	US-2008-0056377- A1	3/6/2008
Method and system for providing error resiliency	11/735,085 4/13/2007		
A system and method of motion vector estimation using content associativity	11/966,095 12/28/07		
Hybrid memory compression scheme for decoder bandwidth reduction	11/971,045 01/08/08		
Method and System for Receiving and Framing Packetized Data	09/490,350 01/24/00	6,763,390	07/13/04
Method and System for Receiving and Framing Packetized Data	10/818,812 04/6/04	7,376,692	05/20/08
Method and System for Improved Display Filtering	09/790,955 02/22/01	6,710,819	03/23/04

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Title	Application Number/ Filing Date	Pub. No./ Patent No.	Pub. Date/ Issue Date
Method and Apparatus for Processing Video and Graphics Data	09/923,516 080/7/01	6,828,987	12/07/04
Tiled Memory Configuration for Mapping Video Data and Method Thereof	09/923,520 08/07/01	7,016,418	02/21/06
System For Testing Multiple Devices on a Single System and Method Thereof	09/923,524 08/07/01	7,253,818	080/7/07
Memory Controller for Handling Multiple Clients and Method Thereof	11/627,585 01/26/07	2007/0124793 A1	05/31/07
Method and System for Accessing Packetized Elementary Stream Data	09/489,682 01/24/00	6,778,533	08/17/04
Method and System for Retrieving Adaptation Field Data Associated with a Transport Packet	09/490,207 01/24/00	6,785,336	08/31/04
Method and Apparatus for Handling Private Data from Transport Stream Packets	09/491,122 01/24/00	6,804,266	10/12/04
Method for Displaying Data	09/489,681 01/24/00	6,999,424	2/14/06
Method and System for Generating Transport Stream Packets	11/333,811 01/17/06	2006/0209709 A1	09/21/06
A Method and System for Handling Errors and a System for Receiving Packet Stream Data	09/489,669 1/24/2000	6,988,238	01/17/06
Method and System for Handling Errors	10/919,943 08/17/04	7,366,961	04/29/08
Method and System for Handling Data Packets	09/791,045 2/22/2001	6,807,585	10/19/04
Method and System for Handling Errors	12/031,584 02/14/08	N/A	N/A
System for Controlling a Clock Signal for Synchronizing a Counter to a Received Value and Method Thereof	09/563,209 5/2/2000	6,674,805	01/06/04
System for Handling compressed Video Data and Method Thereof	09/563,211 5/2/2000	7,113,546	09/26/06
System for Bit-Rate Controlled Digital Stream Playback and Method Thereof	09/800,226 3/6/2001	6,907,481	06/14/05
System for Digitized Audio Stream Synchronization and Method Thereof	09/800,224 3/6/2001	7,030,930	04/18/06

Title	Application Number/ Filing Date	Pub. No./ Patent No.	Pub. Date/ Issue Date
System for Digital Stream Transmission and Method Thereof	09/800,223 03/06/01	7,047,330	05/16/06
System for Frame Based Audio Synchronization and Method Thereof	09/833,493 04/11/01	7,130,316	10/31/06
Method for synchronizing to a data stream	09/491,119 01/24/00	6,885,680	04/26/05
Systems, methods, and apparatus for synchronization of audio and video signals	11/754,096 05/25/2007	20070276670A1	11/29/07
Method and apparatus for deinterlacing video	09/539,572 03/31/2000	6,680,752	01/20/04
Method for deinterlacing interlaced video by a graphics processor	09/553,143 04/20/2000	6,970,206	11/29/05
Diversity receiver with joint signal processing	09/363,813 07/30/1999	6,560,299	05/06/03
Diversity receiver with joint signal processing	10/384,048 03/07/03	6,970,523	11/29/05
Diversity receiver with joint signal processing	10/409,371 04/09/03	6,870,892	03/22/05
Diversity receiver with joint signal processing	10/408,881 04/09/03	6,937,677	08/30/05
Method and apparatus for generating a video overlay	09/678,362 10/03/00	6,788,309	09/07/04
Method and apparatus for reducing instruction dependencies in extended SSA form instructions	10/954,586 09/30/04	2006-0070050	03/30/06
Automatic audio and video synchronization	10/907,073 03/18/05	2006-0209210	09/21/2006

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Title	Application Number/ Filing Date	Pub. No./ Patent No.	Pub. Date/ Issue Date
Receiver for robust data extension for 8VSB signaling	10/251,650 09/20/02	7,194,047	03/20/07
Receiver for robust data extension for 8VSB signaling	11/725,571 03/19/07	2007-237263	10/11/07
Hybrid Soft and Hard Decision Feedback Equalizer	09/549,368 04/14/00	7,006,565	02/28/06
Adaptive Equalizer with Enhanced Error Quantization	09/231,888 01/14/99	6,418,164	07/09/02
Digital Pixel Clock Genera-tion Circuit and Method Employing Independent Clock	10/908,429 05/11/05	2006-0256102	11/16/06
Equalizer method and apparatus using constant modulus algorithm blind equalization and partial decoding	09/457,496 12/09/99	6,668,014	12/23/03
Adaptive equalizer with decision directed constant modulus algorithm	09/261,843 03/03/99	6,337,878	01/08/02
Method and apparatus for encoding video color information	08/761,642 12/06/96	6,124,899	09/26/00
Intra motion prediction for response time compensation	11/864,362 09/28/07		
Response time compression using a complexity value of image information	11/864,391 09/28/07		
Compression Method and Apparatus for Response Time Compensation	11/864,412 09/28/07		
Spread spectrum fifo and method for storing data for multiple display types	09/484,367 01/14/00	6,580,432	06/17/03
Method and apparatus for processing image data	12/144,018		

Title	Application Number/ Filing Date	Pub. No./ Patent No.	Pub. Date/ Issue Date
	06/23/08		
Image processing method and system with repetitive pattern detection	61/129,916 07/29/08		
Adaptation of frame rate converter output target display times based on video content detection	61/071,470 04/30/08		
Method and apparatus for transmitting and using picture descriptive information in a frame rate conversion processor	12/174,738		
Null detection and erasure decoding for frequency selective channel in a broadcasting system	12/143,434		